Optimization of Active Microwave Frequency Multiplier Performance Utilizing Harmonic Terminating Impedances

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Abstract—**A primary factor affecting optimum performance of microwave multipliers employing nonlinear devices is the proper termination of the fundamental and other harmonic frequency components. The objective of this paper is to present a *quantitative* analysis leading to the assessment of optimum terminating impedances in the design of active frequency multipliers with special attention given to harmonics other than those desired. The analysis includes computer modeled HEMT data and supporting measured data for corresponding circuit realizations. Circuit designs are presented utilizing HEMT transistors as the active element to verify modeled results. Based on available literature, the results demonstrate, for the first time, the *quantitative* effects of harmonic termination on active multiplier conversion gain and fundamental and higher harmonic suppression. An experimental design reveals an improvement in multiplier gain of 124% over the conventional approach and data is presented which *quantitatively* illustrates the advantages of impedance termination considerations under optimal bias conditions.**

I. Introduction

NUMEROUS techniques exist for realization of frequency multipliers. At radio frequencies these techniques typically employ a nonlinear device to generate the desired frequency multiple. In the design of passive multipliers, the nonlinear element is typically a varactor diode. In the active case, the nonlinear element typically includes any of several transistor classes such as BJT, FET, etc.

In many frequency multiplier design approaches, the operating performance is improved by the proper selection of input and output circuit terminating impedances at the fundamental and harmonic frequencies [1]–[5]. In the literature there is apparently little substantive in-depth *quantitative* coverage of this topic with *supporting modeled and measured data* for either BJT or FET family realizations [10], [11], [14], [17]–[24]. In the case of HEMT multipliers, coverage of this topic with supporting data is nonexistent. Stancliff [1] and Gilmore [2] state that in order to optimize the response of the FET multiplier, the optimum output load at the *fundamental* frequency is an open circuit shifted by the conjugate of the output capacitance of the FET, but they do not discuss mechanisms or regions. Rauscher [3] has performed a detailed study of doubler performance based on the fundamental frequency drive level, the device output terminating impedance at the fundamental frequency, and the device input terminating impedance at the second harmonic frequency. He concluded that the optimal output load at the fundamental frequency was a short-circuited stub at an optimal distance from the FET drain. The excellent study performed by Rauscher can be strengthened. The FET model used in Rauscher's study used approximations and only simulated data was employed in the conclusion on output termination effects. An experimental circuit built by Rauscher based on his analysis provided responses which required trimming and tuning screws to approximate simulations. In pursuit of optimal performance, it is important that the analysis contain both simulated and measured data. Measured results show the practicality of the designs and the accuracy of the models which contain approximations. Camargo [4], [9], [16], who appears to have performed the most in-depth research in this area, concluded that optimum MESFET doubler operation is obtained when the drain is terminated at the fundamental frequency by a purely reactive circuit which resonates the transistor's output capacitance, while Borg [5] suggests that the optimum terminating impedance for a bipolar multiplier is a short circuit at the fundamental frequency. Many authors, however, do not give substantial quantitative attention to regions of nonlinearity, terminating impedance, or spectral purity.

This paper presents a *quantitative* analysis of the optimization of active multiplier conversion gain and spectral purity as governed by fundamental and harmonic terminating impedances and regions of nonlinearity. It is believed that access to this quantitative information will be of use for designers of future circuits. HEMT transistors are employed to represent the class of nonlinear element to illustrate the approach. The optimum terminating impedances are determined for the input and output ports of the active device utilizing a recent nonlinear circuit model for HEMT transistors. This is in marked contrast with earlier studies which used approximations in the simulated performance predictions [2], [3], [9], [14]. In the nonlinear model used by Rauscher [3], for example, fixed values for the gate-to-source capacitance (C_{gs}) and gate-to-drain capacitance (C_{gd}) were used. In the simulation process, he has assumed, for higher harmonic matching conditions, that the input and output terminating impedances are zero for third-order and higher harmonics. The nonlinear model employed by Camargo [9] uses fixed values for all elements except the transconductance (g_m) and output conductance (g_d), and according to the author, does

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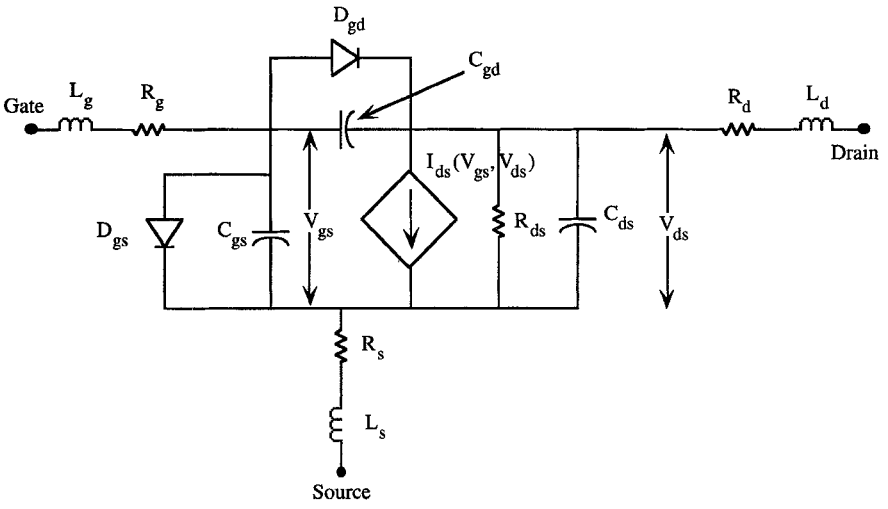

Fig. 1. HEMT nonlinear equivalent model.

not employ gate-to-drain capacitance (C_{gd}) nonlinearity. The results presented in this work incorporate dependencies between the input and output harmonic terminating impedances which are not found in preceeding studies. For the multipliers examined in this paper, these impedances include terminations at the fundamental, second harmonic, and third harmonic frequencies. Measured data are presented which validate the practicality of the designs and the accuracy of the simulations.

II. Nonlinear Model

Fig. 1 is a circuit model for the class of nonlinear active devices being considered in this paper. The case of the MESFET is considered initially to introduce essential concepts which, of course, are relatable to the HEMT case. In analyzing FET performance, it has been found that the elements which contribute to the nonlinear behavior are the drain-source current I_{ds}, the gate-source capacitance C_{gs}, gate-drain capacitance C_{gd}, output resistance R_{ds}, and diodes D_{gs} and D_{gd} (Fig. 1) [3], [4], [6]–[12]. From the construction of plots showing variations of device elements as a function of bias voltage, it may be observed that the aforementioned parameters showing the greatest nonlinearity are the transconductance g_m, gate-source capacitance C_{gs}, gate-drain capacitance C_{gd}, and output resistance R_{ds}, with the dominant nonlinear circuit elements being g_m and R_{ds} [3], [6], [8], [12]. Maas [12] demonstrates this by analyzing a nonlinear model of a MESFET. In his study, values are given for all parasitic components ($L_s, L_g, L_d, R_g, R_s, R_d$) and intrinsic circuit components ($R_i, R_{ds}, C_{gs}, C_{gd}$, and g_m) for various control voltages and this data qualitatively illustrates those elements which possess the strongest nonlinearities.

For the class of multipliers under consideration, the nonlinear behavior of the drain-to-source current (I_{ds}) produces harmonic generation through its clipping effect [9], [14]. In the case of harmonic generation, the conclusion has been advanced that optimum harmonic generation occurs for either $V_{gs} = 0$ or $V_{gs} = V_p$ [7], [9]. If the FET is biased at $V_{gs} = 0$, the input voltage waveform appearing across the gate-to-source capacitance (C_{gs}) is clipped and will be half-wave rectified due to the conduction cycles experienced by the gate-to-source diode. This rectified waveform is transferred to I_{ds} through the device's transfer properties as reflected by the analytical relation between I_{ds} and V_{gs}. When the device is biased at the pinchoff voltage ($V_{gs} = V_p$), however, the input voltage at the gate causes the FET to turn on during the positive half-cycle of the input voltage and the output voltage again becomes a half-wave rectified waveform. When the gate voltage is biased between 0 volts and the pinchoff voltage ($0 \geq V_{gs} \geq V_p$), and the input voltage swing is large enough to cause clipping on both ends, the output current at the drain will resemble a square wave. If the square wave is symmetrical, the second harmonic component will be small but the third harmonic is large allowing frequency tripling [8].

Focusing on the HEMT case, Golio [6] has performed an analysis with a HEMT utilizing measured data for I_{ds}, output resistance R_{ds}, transconductance g_m, gate-source capacitance C_{gs}, and gate-drain capacitance C_{gd} as a function of bias voltage. Based on the measured components corresponding to the parameters of the HEMT model as functions of the bias voltages, it has been determined that the strongest nonlinearities are R_{ds} and I_{ds} [6], [12].

Based on the device nonlinearities described, it has been found [6] that the transconductance is most critical to the accurate prediction of many large-signal effects. Using the Curtice HEMT model, the transconductance,[1] output conductance, and drain-to-source current of the HEMT device may be expressed as in [6], as shown in the equation at the bottom of the next page, where

$f(V_{ds}) = \tanh(\alpha V_{ds})(1 + \lambda V_{ds})$;

V_{pf} voltage at which transconductance begins to degrade from that of a FET;

δ, ψ empirical transconductance degradation parameters;

β empirical transconductance parameters;

α empirical saturation factor;

λ empirical output conductance factor.

[1] The transductance of the MESFET and HEMT exhibit similar behavior up to a certain gate voltage. In contrast to the MESFET, however, the HEMT transconductance begins to decrease rapidly at some gate bias level (V_{pf}). Thus, the analytical expression for the MESFET has to be altered to model the transconductance of the HEMT.

The basic nonlinear model of the Fujitsu FHX35LG HEMT employed in this paper is shown in Fig. 1 (case parasitics are included in the model but not shown in the figure). Static I-V curves for this HEMT, obtained from the model of Fig. 1 and laboratory measurements [see Fig. 2(a)], are employed to characterize two dominant circuit element nonlinearities: transconductance (g_m) and the output conductance (g_d). These parameters (modeled *and* measured), which were derived from the above sources, are plotted versus the drain-to-source (V_{ds}) and gate-to-source (V_{gs}) voltages shown in Fig. 2(a)–(e). These plots graphically display the nonlinearity of the corresponding HEMT elements as a function of the dc bias voltages. This is further explored in the following paragraphs.

In this paper, high efficiency harmonic generation is shown to result for Class A and Class B operation of the HEMT. Class A operation occurs for $V_{gs} \approx 0$ and causes drain current (I_{ds}) rectification when the gate diode swings into forward conduction. Class B operation occurs for $V_{gs} = V_p$ and causes the drain current to clip when the gate voltage swings below pinch-off. It has been stated in some previous studies that Class A FET multipliers provide good multiplication gain and poor DC to RF efficiency while Class B FET multipliers have poor multiplication gain and good DC to RF efficiency [8], [11], [15]. The conclusions for the HEMT multiplier are presented quantitatively in section III.

Utilizing the HEMT transconductance and output conductance plots of Fig. 2(b)–(e), we are able to identify the prominent nonlinear regions for the optimum dc bias points (either $V_{gs} = 0$ or $V_{gs} = V_p$). From these curves the prominent nonlinear regions for $V_{gs} \approx 0$ are Region I of Fig. 2(d) where g_d is dominant and for $V_{gs} = V_p$, Region II of Fig. 2(c) with g_m showing the dominant effect. In the absense of embedding circuitry constraints, a preliminary conclusion on opitmal HEMT multiplier terminating impedances may be drawn at this juncture. If *fundamental* frequency load lines are constructed for these regions, it is seen that Region I requires an open-circuit impedance which allows a maximum V_{ds} voltage swing and Region II requires a short-circuit impedance which allows a maximum I_{ds} current swing. Using the static HEMT *IV* curves, fundamental frequency load lines may be constructed to qualitatively illustrate the optimum terminating load impedance for the fundamental frequency signal. This form of analysis indicates that the optimum impedance for Region I ($V_{gs} = 0$) is an open-circuit impedance which allows a maximum V_{ds} voltage swing. Similarly, the fundamental load line analysis for Region II ($V_{gs} = V_p$) indicates that the optimum impedance is a short-circuit impedance which allows a maximum I_{ds} current swing. These qualitative assertions will be substantiated *quantitatively* in the ensuing discussion.

The HEMT is a square law device which cannot generate harmonic components of just any order. This device, operated entirely in its square-law region, can be used for frequency doubling, but will produce a third harmonic frequency if the second harmonic output signal feeds back to the input and mixes in the device with the input fundamental signal [2]. As an example, consider the HEMT with the drain-to-source current for $V_{gs} \leq V_{pf}$ represented as [6]

$$I_{ds} = \beta(V_{gs} - V_p)^2 f(V_{ds}). \tag{1}$$

Allowing the input voltage to consist of the input fundamental signal and the second harmonic reflected back to the input of the device:

$$V_{gs} = A_1 \cos\omega_o t + A_2 \cos(2\omega_o t + \theta) \tag{2}$$

where A_1 is the amplitude of the fundamental signal, A_2 is the amplitude of the reflected second harmonic, ω_o is the fundamental frequency, and θ is the phase angle of the reflected second harmonic. Utilizing (2) in the expression for I_{ds} reveals that frequency components are obtained at dc, $\omega_o, 2\omega_o, 3\omega_o$ and $4\omega_o$, and the component at $2\omega_o$ can be enhanced or degraded by the reflected signal.

III. Optimal Design

The above analysis provides motivation for development of an optimal design approach. Toward this end, a specific illustrative multiplier design is employed as a vehicle. The basic topology of the frequency multiplier utilized in this paper is illustrated in Fig. 3. In this configuration, $SC_i; i = 1, M$ and $OC_j; j = 1, N$ represent short-circuit and open circuit terminating impedances, respectively, for the multiplier input network at the respective frequencies. Similarly, $SC_k; k = 1, O$ and $OC_l; l = 1, P$ represent short and open-circuit terminating impedances for the multiplier output network. An infinite number of circuit realizations exist which conform

$$g_m = \begin{cases} 0, & V_{gs} \leq V_p \\ 2\beta(V_{gs} - V_p) f(V_{ds}), & V_{gs} \leq V_{pf} \\ 2\beta(V_{gs} - V_p) f(V_{ds}) \delta(V_{gs} - V_{pf}), & V_{gs} > V_{pf} \end{cases}$$

$$g_d = \begin{cases} \beta(V_{gs} - V_p)^2(1 + \lambda V_{ds})(\alpha/\cosh^2(\alpha V_{ds})) + \beta(V_{gs} - V_p)^2 \lambda \tanh(\alpha V_{ds}), & V_{gs} \leq V_{pf} \\ \beta(V_{gs} - V_p)^2(1 + \lambda V_{ds})(\alpha/\cosh^2(\alpha V_{ds})) + \beta(V_{gs} - V_p)^2 \lambda \tanh(\alpha V_{ds}), & \\ \quad -\dfrac{\delta}{\psi + 1}(V_{gs} - V_{pf})^{\psi+1} \dfrac{df(V_{ds})}{dV_{ds}}, & V_{gs} > V_{pf} \end{cases}$$

$$I_{ds} = \begin{cases} 0, & V_{gs} \leq V_p \\ \beta(V_{gs} - V_p)^2 f(V_{ds}), & V_{gs} \leq V_{pf} \\ \beta(V_{gs} - V_p)^2 f(V_{ds}) - \dfrac{\delta}{\psi + 1}(V_{gs} - V_{pf})^{\psi+1} f(V_{ds}), & V_{gs} > V_{pf} \end{cases}$$

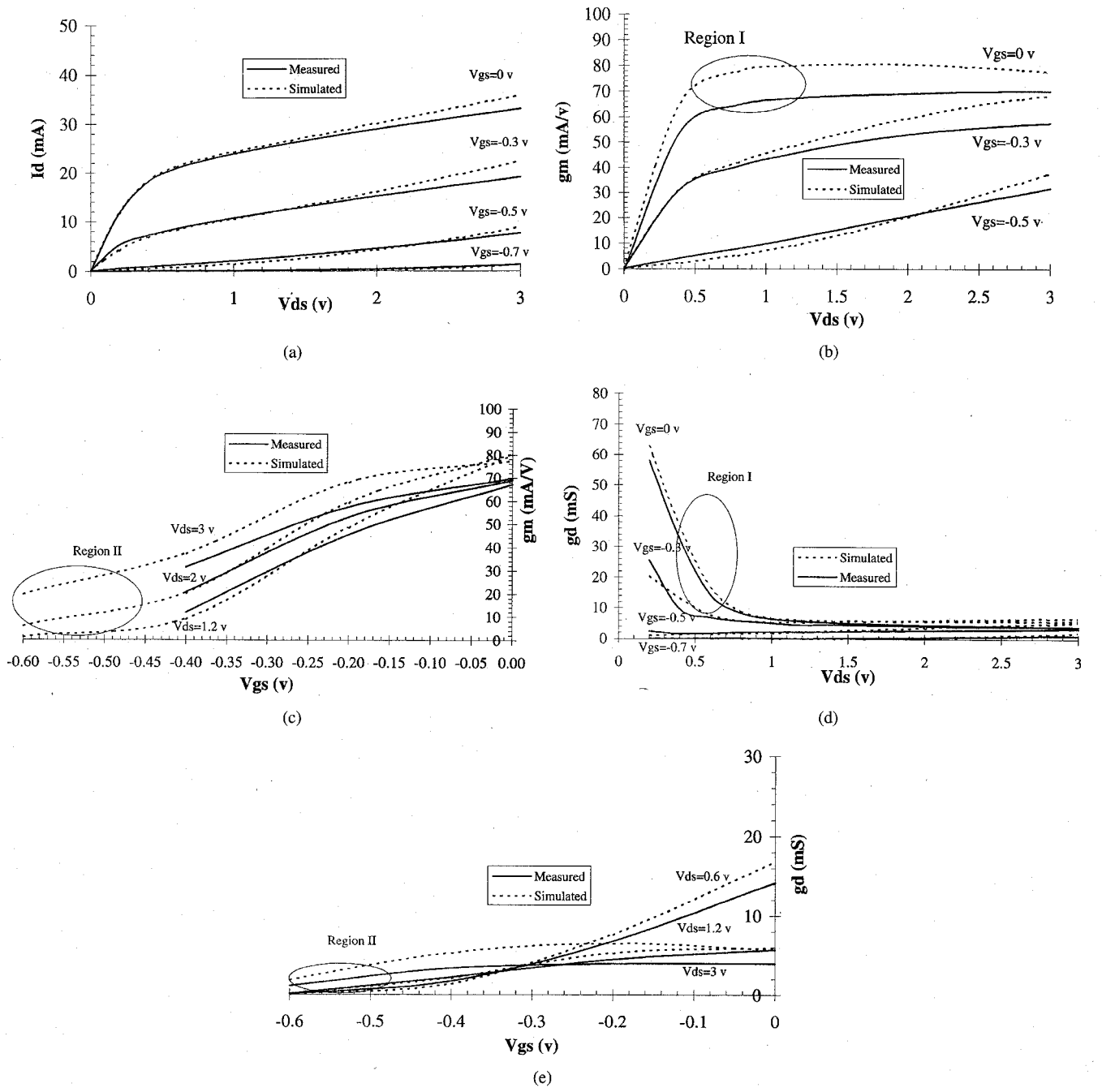

Fig. 2. (a) Measured and simulated *IV* curves of FHX35LG HEMT transistor. (b) Measured and simulated transconductance (g_m) of FHX35LG. (c) measured and simulated transconductance (g_m) of FHX35LG. (d) Measured and simulated conductance (g_d) of FHX35LG. (e) Measured and simulated output conductance (g_d) of FHX35LG.

to the configuration of Fig. 3. This provides the motivation for construction of a matrix of various circuit configurations as illustrated in Table I which displays various harmonic terminating impedances on the input and output ports of the multiplier realization depicted in Fig. 3. Tables have been constructed for multiplier operation (up to the third harmonic) utilizing the precision HEMT computer model with case parasitics which was discussed earlier. With reference to Table I, the left-hand vertical column represents various impedance terminations of the input network at the fundamental, second harmonic, and third harmonic frequencies. The top horizontal row represents various impedances of the output network at the fundamental, second harmonic, and third harmonic frequencies.

To assess performance under various load terminations several load configurations were analyzed. Based on previous discussions, fundamental and harmonic loads of interest fall into several categories: these loads may be short-circuited, open-circuited, matched or 50 ohms.

As a first case, the options shown in Table I were selected. Since only 50 ohms, short and open loads are used, this choice of terminations would appear to provide a concrete basis for assessing the effects of a variety of other input and output harmonic load conditions. Table I illustrates the conversion

TABLE I
REGION II RESPONSES TO VARIOUS HARMONIC TERMINATIONS (LUMPED COMPONENTS, $V_{gs} = -0.7\,\text{v}, V_{ds} = 3\,\text{v}, P_{\text{in}} = 0\,\text{dBm}$)

	OUTPUT NETWORK																	
	50 ohm @ fo		short circuit @ fo		open circuit @ fo		short circuit @ fo		open circuit @ fo		50 ohm @ fo		50 ohm @ fo		short circuit @ fo		open circuit @ fo	
	50 ohm @ 2fo		50 ohm @ 2fo		50 ohm @ 2fo		50 ohm @ 2fo		50 ohm @ 2fo		50 ohm @ 2fo		50 ohm @ 2fo		50 ohm @ 2fo		50 ohm @ 2fo	
INPUT NETWORK	50 ohm @ 3fo		50 ohm @ 3fo		50 ohm @ 3fo		open circuit @ 3fo		open circuit @ 3fo		short circuit @ 3fo		open circuit @ 3fo		short circuit @ 3fo		short circuit @ 3fo	
	Output Power (dBm)		Output Power (dBm)		Output Power (dBm)		Output Power (dBm)		Output Power (dBm)		Output Power (dBm)		Output Power (dBm)		Output Power (dBm)		Output Power (dBm)	
50 ohm @ fo	Po @ fo	5.96	Po @ fo	-73	Po @ fo	-66.5	Po @ fo	-73.2	Po @ fo	-66.5	Po @ fo	5.9	Po @ fo	5.9	Po @ fo	-73.2	Po @ fo	-66.5
50 ohm @ 2fo	Po@2fo	-0.9	Po@2fo	0	Po@2fo	-1	Po@2fo	0.3	Po@2fo	-0.7	Po@2fo	-1.3	Po@2fo	-0.7	Po@2fo	-0.2	Po@2fo	-1.4
50 ohm @ 3fo	Po@3fo	-14.7	Po@3fo	-14	Po@3fo	-17.8	Po@3fo	-72.5	Po@3fo	-107	Po@3fo	-94	Po@3fo	-104	Po@3fo	-94	Po@3fo	-97.2
50 ohm @ fo	Po @ fo	6.2	Po @ fo	-72.9	Po @ fo	-66.3	Po @ fo	-72.8	Po @ fo	-66.3	Po @ fo	6.2	Po @ fo	6.3	Po @ fo	-72.9	Po @ fo	-66.3
short circuit @ 2fo	Po@2fo	0.3	Po@2fo	1.5	Po@2fo	-0.1	Po@2fo	1.8	Po@2fo	0.2	Po@2fo	0	Po@2fo	0.7	Po@2fo	1.2	Po@2fo	-0.5
50 ohm @ 3fo	Po@3fo	-11.8	Po@3fo	-10.6	Po@3fo	-17.2	Po@3fo	-68.9	Po@3fo	-106	Po@3fo	-92	Po@3fo	-100	Po@3fo	-91.1	Po@3fo	-97.7
50 ohm @ fo	Po @ fo	6	Po @ fo	-72.9	Po @ fo	-66.3	Po @ fo	-72.8	Po @ fo	-66.5	Po @ fo	6.2	Po @ fo	6.3	Po @ fo	-72.9	Po @ fo	-66.3
short circuit @ 2fo	Po@2fo	-1.2	Po@2fo	1.5	Po@2fo	-0.1	Po@2fo	1.8	Po@2fo	-0.9	Po@2fo	0.3	Po@2fo	0.7	Po@2fo	1.2	Po@2fo	-0.5
short circuit @ 3fo	Po@3fo	-13.4	Po@3fo	-10.6	Po@3fo	-17.2	Po@3fo	-99.1	Po@3fo	-109.6	Po@3fo	-11.8	Po@3fo	-100.6	Po@3fo	-91.1	Po@3fo	-97.7
50 ohm @ fo	Po @ fo	5.9	Po @ fo	-73.2	Po @ fo	-66.5	Po @ fo	-73.2	Po @ fo	-66.5	Po @ fo	5.9	Po @ fo	5.9	Po @ fo	-73.2	Po @ fo	-66.7
50 ohm @ 2fo	Po@2fo	-2.2	Po@2fo	-1.3	Po@2fo	-2.3	Po@2fo	-1.2	Po@2fo	-1.7	Po@2fo	-1.3	Po@2fo	-2.1	Po@2fo	-0.1	Po@2fo	-2.7
short circuit @ 3fo	Po@3fo	-17.1	Po@3fo	-16.8	Po@3fo	-15.8	Po@3fo	-108.2	Po@3fo	-106.6	Po@3fo	-94.5	Po@3fo	-108	Po@3fo	-94.1	Po@3fo	-90.5
50 ohm @ fo	Po @ fo	6.1	Po @ fo	-73	Po @ fo	-66.6	Po @ fo	-73.1	Po @ fo	-66.6	Po @ fo	6.1	Po @ fo	6.1	Po @ fo	-73	Po @ fo	-66.5
open circuit @ 2fo	Po@2fo	-1	Po@2fo	0	Po@2fo	-1.2	Po@2fo	0.1	Po@2fo	-1	Po@2fo	-1.1	Po@2fo	-0.8	Po@2fo	-0.2	Po@2fo	-1.5
50 ohm @ 3fo	Po@3fo	-15.9	Po@3fo	-15.3	Po@3fo	-21.2	Po@3fo	-104	Po@3fo	-109	Po@3fo	-96	Po@3fo	-105	Po@3fo	-96.1	Po@3fo	-100.4
50 ohm @ fo	Po @ fo	6.1	Po @ fo	-73	Po @ fo	-66.5	Po @ fo	-73	Po @ fo	-66.5	Po @ fo	6.1	Po @ fo	6.1	Po @ fo	-73	Po @ fo	-66.5
open circuit @ 2fo	Po@2fo	-0.9	Po@2fo	0	Po@2fo	-1.1	Po@2fo	0.3	Po@2fo	-0.9	Po@2fo	-1.2	Po@2fo	-0.7	Po@2fo	-0.2	Po@2fo	-1.4
open circuit @ 3fo	Po@3fo	-15.7	Po@3fo	-15.1	Po@3fo	-20	Po@3fo	-104	Po@3fo	-108	Po@3fo	-96.2	Po@3fo	-105	Po@3fo	-96	Po@3fo	-99.8
50 ohm @ fo	Po @ fo	6	Po @ fo	-73.1	Po @ fo	-66.5	Po @ fo	-73	Po @ fo	-66.5	Po @ fo	6	Po @ fo	6	Po @ fo	-73	Po @ fo	-66.5
50 ohm @ 2fo	Po@2fo	-0.8	Po@2fo	0.1	Po@2fo	-0.9	Po@2fo	0.4	Po@2fo	-0.7	Po@2fo	-1.3	Po@2fo	-0.5	Po@2fo	-0.2	Po@2fo	-1.4
open circuit @ 3fo	Po@3fo	-14.3	Po@3fo	-13.6	Po@3fo	-17	Po@3fo	-102	Po@3fo	-105	Po@3fo	-94.4	Po@3fo	-103	Po@3fo	-93.9	Po@3fo	-96.9

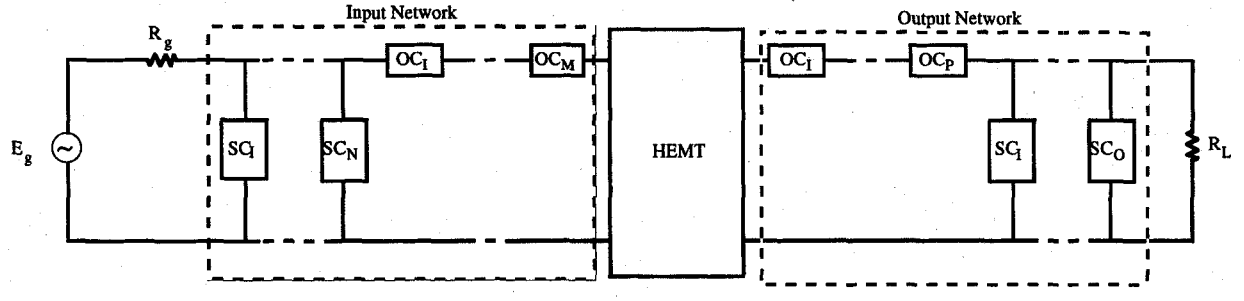

Fig. 3. Frequency multiplier realization.

gains obtained employing the FHX35LG HEMT utilizing a Harmonic Balance program with input and output networks synthesized with lumped elements to realize the indicated harmonic terminations with $f_o = 3$ GHz. The HEMT in this table is biased at pinchoff $V_{gs} = V_p$ and driven with 0 dbm at the gate terminal (Region II). This table is presented as a basis with which to measure the quantitative impact of a variety of terminations on multiplier conversion gain. The numbers to the right of each entry in the table represent the powers obtained at respective harmonics. It is instructive to consider a typical entry of interest in this table. The entry located in the second row and second column, for example, shows that a conversion gain of 1.5 dB is obtained if the input network terminates the fundamental f_o and third harmonic $3f_o$ in 50 ohms while the second harmonic $2f_o$ is short-circuited. The output network for this entry terminates the fundamental in a short circuit and all other harmonics in 50 ohms. Several authors [3], [9], [11], [16] have reported that the input network should terminate the second harmonic in a short circuit. For lumped input circuit realizations, however, this table reveals that this provides a 1.5 dB improvement over a 50 ohm or an open circuit termination at $2f_o$ (row 1, column 2 and row 5, column 2 respectively). While the conversion gains represented in *this* table are not large and the db values do not show great variation, several trends are seen to emerge and subsequent results will substantiate their implications. In particular, the impact of *input* network terminations show from the data in rows 2 and 3, that for doubler operation, a short circuit termination at $2f_o$ provides the best conversion gain in all cases considered.

Furthermore, a perusal of output network termination responses show that a short circuit at f_o provides the best performance using conversion gain as a basis.

A similar table was developed for the case where the HEMT is biased at $V_{gs} = 0$ (Region I). This V_{gs} value was chosen in accordance with our previous discussion on optimum bias regions. While an important outcome of the $V_{gs} = 0$ table (not shown) was typically lower conversion gains in comparison with Table I where $V_{gs} = V_p$, an even more significant observation is the dramatic improvement ($\sim$12 dB) obtained by employing an *open* circuit termination at f_o in the output network, in contrast with a short circuit as was the optimum case for Region II. Note that Table I predicts only a 1.6 dB improvement for the analogous comparison.

Based on these results and the author's detailed studies for other cases, only results will be presented for the specific case where the input network is short-circuited at $2f_o$ in the ensuing discussion.

TABLE II
REGION II RESPONSES TO VARIOUS HARMONIC TERMINATIONS WITH INPUT MATCHED AT f_o (LUMPED COMPONENTS, $V_{gs} = -0.7\,\text{v}, V_{ds} = 3\,\text{v}, P_{\text{in}} = 0\,\text{dBm}$)

	OUTPUT NETWORK																	
	50 ohm @ fo		short circuit @ fo		open circuit @ fo		short circuit @ fo		open circuit @ fo		50 ohm @ fo		50 ohm @ fo		short circuit @ fo		open circuit @ fo	
	50 ohm @ 2fo		50 ohm @ 2fo		50 ohm @ 2fo		50 ohm @ 2fo		50 ohm @ 2fo		50 ohm @ 2fo		50 ohm @ 2fo		50 ohm @ 2fo		50 ohm @ 2fo	
INPUT NETWORK	50 ohm @ 3fo		50 ohm @ 3fo		50 ohm @ 3fo		open circuit @ 3fo		open circuit @ 3fo		short circuit @ 3fo		open circuit @ 3fo		short circuit @ 3fo		short circuit @ 3fo	
	Output Power (dBm)		Output Power (dBm)		Output Power (dBm)		Output Power (dBm)		Output Power (dBm)		Output Power (dBm)		Output Power (dBm)		Output Power (dBm)		Output Power (dBm)	
50 ohm @ fo	Po @ fo	5.96	Po @ fo	-217	Po @ fo	-210	Po @ fo	-215	Po @ fo	-208	Po @ fo	5.5	Po @ fo	4.1	Po @ fo	-216	Po @ fo	-209
50 ohm @ 2fo	Po@2fo	-0.9	Po@2fo	-0.3	Po@2fo	-0.7	Po@2fo	0.2	Po@2fo	0.4	Po@2fo	-3.9	Po@2fo	0.3	Po@2fo	-3.3	Po@2fo	-4.2
50 ohm @ 3fo	Po@3fo	-14.7	Po@3fo	-221	Po@3fo	-231	Po@3fo	-270	Po@3fo	-270	Po@3fo	-232	Po@3fo	-237	Po@3fo	-270	Po@3fo	-270
	Output Power (dBm)		Output Power (dBm)		Output Power (dBm)		Output Power (dBm)		Output Power (dBm)		Output Power (dBm)		Output Power (dBm)		Output Power (dBm)		Output Power (dBm)	
Matched @ fo	Po @ fo	14.4	Po @ fo	-65.7	Po @ fo	-62.3	Po @ fo	-65.7	Po @ fo	-62.5	Po @ fo	13	Po @ fo	13	Po @ fo	-65.6	Po @ fo	-62.2
short circuit @ 2fo	Po@2fo	6.4	Po@2fo	8	Po@2fo	5	Po@2fo	8.6	Po@2fo	5.2	Po@2fo	6.1	Po@2fo	6.9	Po@2fo	7.4	Po@2fo	4.8
54 ohms @ 3fo	Po@3fo	-2.9	Po@3fo	-4.1	Po@3fo	-7.9	Po@3fo	-92.1	Po@3fo	-92.2	Po@3fo	-87.6	Po@3fo	-94.9	Po@3fo	-84.7	Po@3fo	-92.6

TABLE III
REGION II RESPONSES TO VARIOUS HARMONIC TERMINATIONS WITH INPUT MATCHED AT f_o AND OUTPUT MATCHED AT $2f_o$ (LUMPED COMPONENTS, $V_{gs} = -0.7\,\text{v}, V_{ds} = 3\,\text{v}, P_{\text{in}} = 0\,\text{dBm}$)

	OUTPUT NETWORK																	
	50 ohm @ fo		short circuit @ fo		open circuit @ fo		short circuit @ fo		open circuit @ fo		36 ohms @ fo		37 ohms @ fo		short circuit @ fo		open circuit @ fo	
	50 ohm @ 2fo		Matched @ 2fo		Matched @ 2fo		Matched @ 2fo		Matched @ 2fo		Matched @ 2fo		Matched @ 2fo		Matched @ 2fo		Matched @ 2fo	
INPUT NETWORK	50 ohm @ 3fo		85 ohms @ 3fo		85 ohms @ 3fo		open circuit @ 3fo		open circuit @ 3fo		short circuit @ 3fo		open circuit @ 3fo		short circuit @ 3fo		short circuit @ 3fo	
	Output Power (dBm)		Output Power (dBm)		Output Power (dBm)		Output Power (dBm)		Output Power (dBm)		Output Power (dBm)		Output Power (dBm)		Output Power (dBm)		Output Power (dBm)	
Matched @ fo	Po @ fo	14.4	Po @ fo	-70.2	Po @ fo	-61.9	Po @ fo	-70	Po @ fo	-61.5	Po @ fo	12.8	Po @ fo	12.5	Po @ fo	-70	Po @ fo	-60.6
short circuit @ 2fo	Po@2fo	6.4	Po@2fo	10.1	Po@2fo	4.7	Po@2fo	10.4	Po@2fo	5	Po@2fo	9.1	Po@2fo	7.3	Po@2fo	9.5	Po@2fo	5.1
54 ohms @ 3fo	Po@3fo	-2.9	Po@3fo	-8.1	Po@3fo	-16.2	Po@3fo	-89.5	Po@3fo	-99.1	Po@3fo	-95.8	Po@3fo	-86.1	Po@3fo	-96.7	Po@3fo	-110.3

TABLE IV
SIMULATED DOUBLER RESPONSE WITH MICROSTRIP ELEMENTS (REGION II, $V_{gs} = -0.7\,\text{v}, V_{ds} = 3\,\text{v}, P_{\text{in}} = 0\,\text{dBm}$)

	OUTPUT NETWORK											
	50 ohm @ fo		short circuit @ fo		open circuit @ fo		short circuit @ fo		open circuit @ fo		27 ohms @ fo	
	50 ohm @ 2fo		50 ohm @ 2fo		50 ohm @ 2fo		62 ohms @ 2fo		63 ohms @ 2fo		49 ohms @ 2fo	
INPUT NETWORK	50 ohm @ 3fo		repeat sc @ 3fo		repeat oc @ 3fo		short circuit @ 3fo		open circuit @ 3fo		open circuit @ 3fo	
	Output Power (dBm)		Output Power (dBm)		Output Power (dBm)		Output Power (dBm)		Output Power (dBm)		Output Power (dBm)	
50 ohm @ fo	Po @ fo	5.96	Po @ fo	-27.1	Po @ fo	-10.4	Po @ fo	-25	Po @ fo	-17.3	Po @ fo	4
50 ohm @ 2fo	Po@2fo	-0.9	Po@2fo	-0.7	Po@2fo	-0.9	Po@2fo	0.4	Po@2fo	0.8	Po@2fo	0.6
50 ohm @ 3fo	Po@3fo	-14.7	Po@3fo	-26.3	Po@3fo	-36.2	Po@3fo	-52.9	Po@3fo	-60.1	Po@3fo	-37.7
50 ohm @ fo	Po @ fo	10.7	Po @ fo	-27.4	Po @ fo	-22	Po @ fo	-20.5	Po @ fo	-13.5	Po @ fo	9
short circuit @ 2fo	Po@2fo	4.3	Po@2fo	5.4	Po@2fo	4.5	Po@2fo	8.6	Po@2fo	6.4	Po@2fo	7.2
50 ohm @ 3fo	Po@3fo	-10.2	Po@3fo	-22.6	Po@3fo	-21	Po@3fo	-42.8	Po@3fo	-61	Po@3fo	-32

TABLE V
SIMULATED DOUBLER RESPONSE WITH MICROSTRIP ELEMENTS (REGION I, $V_{gs} = 0\,\text{v}, V_{ds} = 3\,\text{v}, P_{\text{in}} = 0\,\text{dBm}$)

	OUTPUT NETWORK											
	50 ohm @ fo		short circuit @ fo		open circuit @ fo		short circuit @ fo		open circuit @ fo		27 ohms @ fo	
	50 ohm @ 2fo		50 ohm @ 2fo		50 ohm @ 2fo		62 ohms @ 2fo		63 ohms @ 2fo		49 ohms @ 2fo	
INPUT NETWORK	50 ohm @ 3fo		repeat sc @ 3fo		repeat oc @ 3fo		short circuit @ 3fo		open circuit @ 3fo		open circuit @ 3fo	
	Output Power (dBm)		Output Power (dBm)		Output Power (dBm)		Output Power (dBm)		Output Power (dBm)		Output Power (dBm)	
50 ohm @ fo	Po @ fo	12.5	Po @ fo	-20.2	Po @ fo	-15.1	Po @ fo	-22.9	Po @ fo	-12.5	Po @ fo	11.1
50 ohm @ 2fo	Po@2fo	-10.1	Po@2fo	-11.4	Po@2fo	-2.5	Po@2fo	-10.9	Po@2fo	-4	Po@2fo	-10
50 ohm @ 3fo	Po@3fo	-13.9	Po@3fo	-26.3	Po@3fo	-25.4	Po@3fo	-49.3	Po@3fo	-55.4	Po@3fo	-33.9
50 ohm @ fo	Po @ fo	14.7	Po @ fo	-18.4	Po @ fo	-14.4	Po @ fo	-21.3	Po @ fo	-11.1	Po @ fo	13.2
short circuit @ 2fo	Po@2fo	-12.5	Po@2fo	-13.1	Po@2fo	1.8	Po@2fo	-10.4	Po@2fo	2.8	Po@2fo	-10.6
50 ohm @ 3fo	Po@3fo	-8.4	Po@3fo	-18.4	Po@3fo	-25.6	Po@3fo	-41	Po@3fo	-52	Po@3fo	-2.8

Table II presents the results obtained for Region II operation ($V_{gs} = V_p$) when the input network was synthesized to provide a matched load at the fundamental frequency, f_o, and a short at $2f_o$. In comparison with its counterpart in row 2 of Table I which had a 50 ohm termination at f_o, it is seen that, as expected, significant improvements occur in conversion gains for all output network impedance terminations. A perusal of the values indicate that *significant increases* in conversion gain of over 5 dB are typical in each case. Furthermore, the following quantitative results may be observed for various *output* network terminations: 1) 3.0 dB better conversion gains are obtained due to short circuiting as compared with open circuiting the fundamental (i.e. 8.0 versus 5.0 dB); 2) 1.5 dB better conversion gain will be obtained for a short circuit at f_o in comparison with a 50 ohm termination (notwithstanding the fact that the 50 ohm case would require some form of output circuit fundamental suppression); 3) 1.2 dB of additional conversion gain is obtained if the third harmonic is open circuited in contrast with the frequently used short circuited third harmonic (8.6 versus 7.4 dB); and 4) 3.8 dB additional conversion gain is obtained over the case where an open circuit fundamental and short circuit third harmonic output network are employed (i.e. 8.6 versus 4.8 dB).

Table III presents the results obtained for region II operation when the output network is synthesized to provide a matched load at the second harmonic ($2f_o$) versus the previous cases where a simple 50 ohm load was employed. Based on these results, it can be seen that for output network terminations where the fundamental has been short circuited, an additional $\approx$ 2 dB has been obtained over the results in Table III and approximately 9 dB over Table I results.

Tables IV and V display the results obtained utilizing microstrip line circuits which were synthesized to provide shorted, open, and 50 ohm terminations at respective fundamental and harmonic frequencies as employed in many traditional designs [2]–[5], [8], [9], [13]–[24]. All results are given for an input network synthesized for 50 ohms at f_o, short circuit at $2f_o$ and 50 ohms at $3f_o$.

With reference to Table IV (Region II, $V_{gs} = V_p$), a comparison of the effect of the distributed input network (row

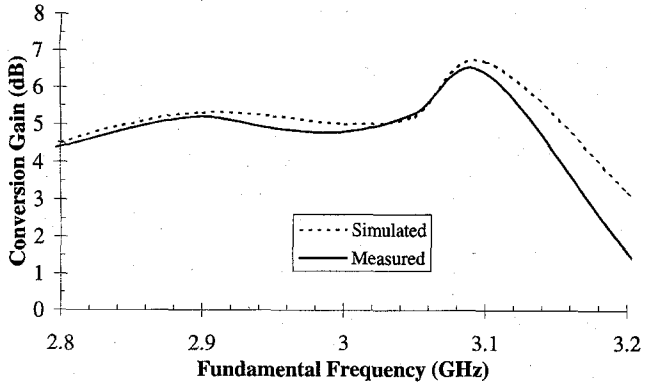

Fig. 4. Conversion gain of output HEMT doubler for traditional design ($P_{\text{in}} = 0\,\text{dBm}, V_{gs} = -0.7\,\text{v}$).

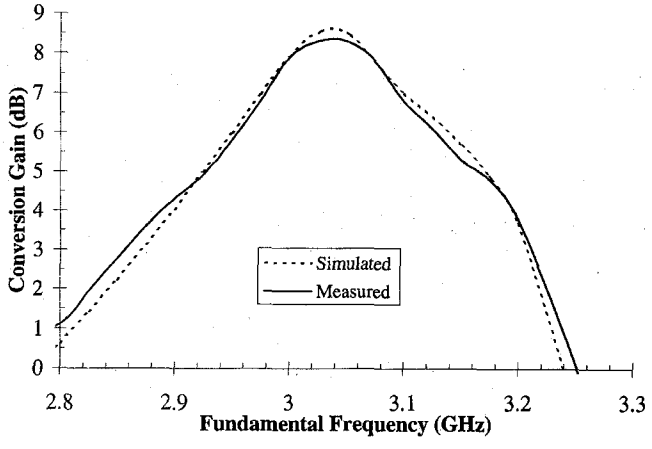

Fig. 5. Conversion gain of HEMT doubler utilizing optimized technique ($P_{\text{in}} = 0\,\text{dBm}, V_{gs} = -0.7\,\text{v}$).

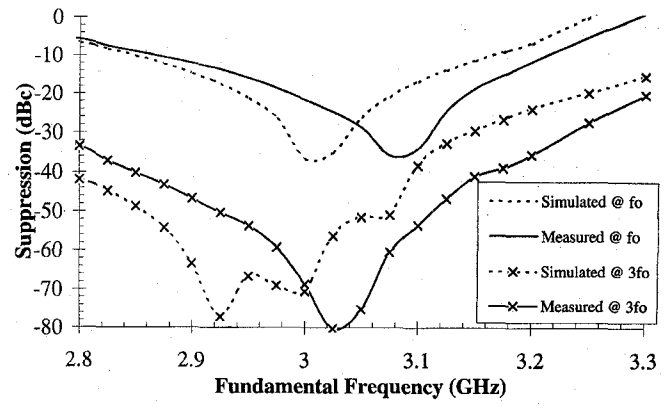

Fig. 6. Harmonic suppression of HEMT doubler utilizing optimized technique ($P_{\text{in}} = 0\,\text{dBm}, V_{gs} = -0.7\,\text{v}$).

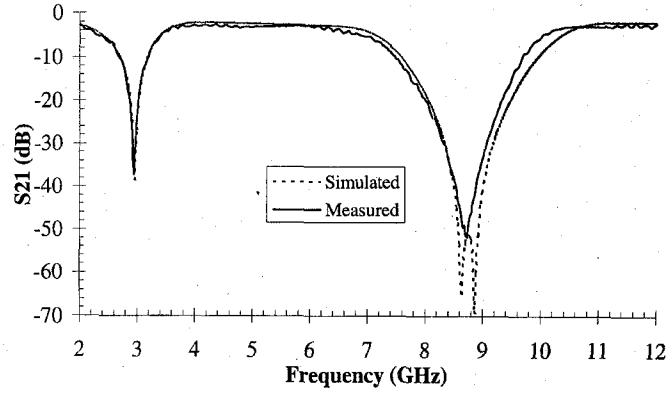

Fig. 7. Transmission magnitude of output network (short circuit @ $f = f_o$ and short circuit @ $f = 3f_o$).

2, column 1) with a 50 ohm input network at $f_o, 2f_o$, and $3f_o$ (row 1, column 1) shows that 5.2 dB improvement in conversion gain performance may be obtained by employing the distributed structure with a short circuit at $2f_o$. Some additional conclusions obtained from a further perusal of this table are as follows: 1) 9.5 dB conversion gain improvement may be obtained by providing a distributed output network which is short circuited at f_o and $3f_o$ as compared with 50 ohm input and output terminations (row 1, column 1 versus row 2, column 4); 2) with the distributed input network terminated in a short circuit 2.2 dB improvement in conversion gain may be obtained by short circuiting the output network at f_o and $3f_o$ (column 4) as compared with open circuits at f_o and $3f_o$ (column 5); 3) the difference in termination in the output network between open and short circuits at f_o is on the order of 1 dB;[2] and 4) an additional 3.2 dB of conversion gain is obtained by introducing an additional short circuited stub at $3f_o$ (row 2, column 2 versus row 2, column 4).

Table V presents similar results for Region I ($V_{gs} = 0$) operation. Several significant conclusions are evident from these results: 1) best performance is considerably less (2.8 versus 8.6 dB) than that for Region II operation; 2) significant conversion gain improvement is obtained when the output network is open circuited at f_o in comparison with the short circuited condition (1.8 versus $-13.1 \approx 15$ dB) (row 2, column 3 versus row 2, column2); and 3) 1 dB of conversion gain performance improvement is achieved by introducing an additional open circuited stub at the third harmonic.

[2]Note that in Tables IV and V the repeat short/open designates the natural periodicity of the distributed input/output networks. Otherwise, a stub has been added at the particular harmonic.

IV. Experimental Results

This section presents experimental results which will corroborate the analysis and conclusions of the previous sections of this paper. A comparison is made between a multiplier designed using a conventional approach and one using the conclusions of this paper.

Several conventional doubler designs have employed a short-circuit termination at the second harmonic frequency on the input network and a short-circuit termination at the fundamental on the output network. The measured and simulated results for the HEMT doubler realization utilizing this conventional approach realized on 20 mil duroid are shown in Fig. 4. This circuit is seen to have a conversion gain of approximately 5 dB around the design doubler center frequency of 3 GHz, rising to 6.7 dB at ≈ 3.1 GHz.

The performance of the frequency doubler designed using the techniques discussed in this paper are shown in Figs. 5 and 6. These figures show the *measured* and *modeled* conversion gain and harmonic suppression versus the fundamental

frequency, respectively. This technique reveals that optimum performance is achieved with the input network terminated with a short circuit at the second harmonic frequency. On the output network, a short circuit at the fundamental frequency, 62 ohms at the second harmonic frequency, and an short circuit termination at the third harmonic frequency yields optimum performance. The transmission $|s_{21}|$ frequency response of this output network is shown in Fig. 7. The resulting implementation of the technique is illustrated in Figs. 5 and 6, where the realized multiplier is seen to have a conversion gain of 8.5 dB, fundamental suppression of $\geq$25 dBc, and third harmonic suppression of $\geq$50 dBc. Comparing Figs. 4 and 5 shows that the optimization approach used in this paper yields and improvement of 3.5 dB in the conversion gain over the conventional doubler realization (1.8 dB if 3.1 GHz is taken for the traditional design).

V. Conclusion

This paper has detailed the results of a comprehensive in-depth study to *quantitatively* determine the effects of passive circuit terminations on microwave active multiplier performance. Subsequent to a discussion of modeled and measured device nonlinearities for the HEMT transistor employed, regions of optimal bias are delineated and employed to quantitatively evaluate multiplier performance. These quantitative results show considerable improvement of frequency multiplier performance (in terms of conversion gain and harmonic suppression) with the addition of proper terminating impedances. The optimizing technique shown in this paper demonstrates the importance of analyzing harmonic terminating impedances with special emphasis on higher-order harmonic terminations which are typically not emphasized in multiplier design and analysis. Modeled results are verified by an experimental design which shows an improvement of 124% over a traditional approach.

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